

AMENDMENTS TO THE CLAIMS

Please amend the claims and add new claims as follows:

1-32. (Cancelled)

1 33. (New) A content addressable memory (CAM) device comprising:
2 a plurality of CAM cells;
3 a first set of compare lines coupled to the plurality of CAM cells to provide a first compare
4 value thereto;
5 a priority encoder to generate a match address; and
6 a second set of compare lines coupled to the plurality of CAM cells and coupled to receive
7 the match address from the priority encoder.

1 34. (New) The CAM device of claim 33 wherein each of the CAM cells includes a first
2 compare circuit coupled to at least one compare line of the first set of compare lines, and a
3 second compare circuit coupled to at least one compare line of the second set of compare
4 lines.

1 35. (New) The CAM device of claim 34 further comprising a first set of match lines coupled
2 to the CAM cells, and a second set of match lines coupled to the CAM cells, and wherein
3 the first compare circuit within each of the CAM cells is coupled to a match line of the first
4 set and the second compare circuit within each of the CAM cells is coupled to a match line
5 of the second set.

1 36. (New) The CAM device of claim 33 wherein the CAM cells are configured to compare
2 data values stored therein simultaneously with the first compare value and with the match

3 address.

1 37. (New) The CAM device of claim 36 further comprising:
2 a first set of match lines coupled to respective rows of the CAM cells to indicate whether
3 the first compare value matches data stored within any of the rows of the CAM cells;
4 and
5 a second set of match lines coupled to the respective rows of the CAM cells to indicate
6 whether the match address matches data stored within any of the rows of the CAM
7 cells.

1 38. (New) The CAM device of claim 33 wherein each of the CAM cells comprises an edge-
2 triggered storage element.

1 39. (New) The CAM device of claim 33 further comprising a plurality of write bit lines
2 coupled to the CAM cells to enable a write data value to be stored within a selected row of
3 the CAM cells.

1 40. (New) The CAM device of claim 39 further comprising a plurality of read bit lines
2 coupled to the CAM cells to enable a read data value to be read from a selected row of the
3 CAM cells.

1 41. (New) The CAM device of claim 33 further comprising a plurality of read word lines
2 coupled to respective rows of the CAM cells to enable a data value to be read from a first
3 selected one of the rows of CAM cells.

1 42. (New) The CAM device of claim 41 further comprising an address circuit to assert at least

2 one of the plurality of read word lines during a sequence of two or more compare
3 operations within the CAM cells.

1 43. (New) The CAM device of claim 41 further comprising a plurality of write word lines
2 coupled to the respective rows of the CAM cells to enable a write data value to be written
3 into a second selected one of the rows of CAM cells concurrently with the read data value
4 being read from the first selected one of the rows of CAM cells.

1 44. (New) The CAM device of claim 43 further comprising an address circuit to concurrently
2 assert one of the plurality of read word lines and one of the plurality of write word lines.

1 45. (New) A method of operation within a content addressable memory (CAM) device, the
2 method comprising:
3 generating a first match address within a priority encoder of the CAM device;
4 outputting the first match address onto a first set of compare lines of a CAM array; and
5 outputting a first compare value onto a second set of compare lines of the CAM array
6 concurrently with outputting the first match address onto the first set of compare
7 lines.

1 46. (New) The method of claim 45 further comprising simultaneously comparing the first
2 match address and the first compare value with contents of the CAM array.

1 47. (New) The method of claim 46 further comprising outputting a data value from the CAM
2 array concurrently with comparing the first match address and the first compare value with
3 contents of the CAM array.

1 48. (New) The method of claim 47 further comprising generating a second match address
2 within the priority encoder after generating the first match address, and comparing the
3 second match address with contents of the CAM array, and wherein outputting the data
4 value from the CAM array comprises outputting the data value from the CAM array for a
5 duration that spans comparison of the match address with contents of the CAM array and
6 comparison of the second match address with contents of the CAM array.

1 49. (New) The method of claim 46 further comprising generating match signals on a first set
2 of match lines to indicate results of comparing the first match address with the contents of
3 the CAM array, and generating match signals on a second set of match lines to indicate
4 results of comparing the first compare value with the contents of the CAM array.

1 50. (New) The method of claim 49 further comprising outputting an error signal if the first
2 match address matches a value stored within the CAM array.

1 51. (New) The method of claim 45 further comprising generating a sequence of check address
2 values within an address generating circuit, and wherein the first compare value is one of
3 the check address values.

- 1 52. (New) A content addressable memory (CAM) device comprising:
 - 2 a CAM array;
 - 3 means for generating a first match address;
 - 4 means for outputting the first match address onto a first set of compare lines of the CAM
 - 5 array; and

6 means for outputting a first compare value onto a second set of compare lines of the CAM
7 array concurrently with outputting the first match address onto the first set of
8 compare lines.

1 53. (New) The CAM device of claim 52 further comprising means for simultaneously
2 comparing contents of the CAM array with the first match address and with the first
3 compare value.

1 54. (New) The CAM device of claim 53 further comprising:
2 means for generating a first set of match signals to indicate results of comparing the first
3 match address with the contents of the CAM array; and
4 means for generating a second set match signals to indicate results of comparing the first
5 compare value with the contents of the CAM array.